a second dielectric layer disposed on the planar dielectric layer and the portions of the borophosphorous silicate glass which are not overlaid by the planar dielectric layer, the layers of undoped silicate glass, borophosphorous silicate glass, planar dielectric layer, and a second dielectric layer together composing a pre-metal dielectric stack.

REMARKS

This Preliminary Amendment, together with the continuation are filed in response to the Final Rejection mailed February 3, 2000. The Examiner objected to claims 1, 4 and 6 for various informalities in the language. In addition, the Examiner rejected claims 1, 3, 4, 9, 10 and 13 for matters relating to form under 35 U.S.C. § 112.

The claims have been amended to overcome the rejection as to matters of informalities and also the matters of form under 35 U.S.C. § 112, second paragraph. Accordingly, the claims should be allowable in this regard.

All claims were rejected over a combination of three prior art references, Kuo in view of applicants' admitted prior art, and further in view of Su et al. Applicants traverse this rejection and believe the claims are patentable in light of this combination of the prior art.

As the Examiner admits, and states, Kuo fails to show a first layer of PETEOS (in the claim, the full phrase is used of "plasma-enhanced tetraethyl orthosilicate"). On top of which is placed a second layer of PETEOS. Indeed, Kuo et al. do not teach or suggest two PETEOS layers, stacked one on top of the other. Neither, of course, is this feature found in applicants' own admitted prior art Figures 1-3. Kuo et al., as well as applicants' admitted prior art also failed to show the additional claimed feature of the first layer of PETEOS being a planarized layer which overlays at least a portion of a BPSG layer and leaves exposed at least some portion of this same BPSG layer so that the second layer of PETEOS overlays and is in direct contact with this BPSG layer. Since neither Kuo et al., nor applicants' admitted prior art planarize the first PETEOS layer by etching until exposing a portion of the BPSG layer, neither of these references can teach nor suggest this claimed feature. Further, neither of these references suggest a yet additional layer of PETEOS on top of the planarized first PETEOS layer which covers both the first PETEOS layer and the exposed portions of the BPSG layer. There are, therefore several

claimed features of claims 1 and 6 which are clearly not found in common or obvious from the two prior art references as combined. The Examiner attempts to rely on Su et al. to supply these missing teachings. Clearly, Su et al. is also deficient in a similar respect and does not supply the teachings which are missing from these two prior art references. First, Su et al. should be understood in the context that Figures 3A and 4A are of the same location, whereas Figures 3B and 4B are not of the same location on the chip and do not directly relate to or attempt to show the same features shown in Figures 3A and 4A. Figures 3B and 4B are not seen even relevant to the present invention since they do not show planarization and removal of material to expose a lower layer. Figures 3A and 4A show planarization of a layer 28 until polysilicon layer 23 is exposed. This polysilicon layer 23 is not a BPSG layer. Further, Su teaches deposition of a first dielectric 27 (a silicon oxide) followed by etching and removal of the dielectric. This is then followed by deposition of a second polysilicon layer which is patterned and etched. After this polysilicon layer is patterned and etched, another dielectric layer 28 is deposited, planarized, then on top of which a further oxide is positioned. This is not seen as relevant to applicants' present invention which has three dielectric layers positioned, one on top of the other before even a first etch is performed and then a fourth dielectric layer is positioned on top thereof. Further, there are no polysilicon layers or pattern and etching of electrical conductors in the middle of the applicants' invention. Su may be summarized as follows: Dielectric 27 formation plus poly 23 deposition plus etch plus dielectric 28 formation plus etch plus dielectric 30 formation. The numbers after each of the layers refer to those layers in Su. As can be seen, each step in Su et al. is followed by some type of etch. There is no example given of three dielectric layers positioned, one on top of the other without etch after which a planarization step takes place. This, indeed is what occurs with applicants' invention and creates the final structure as claimed in claim 1. In particular, applicants' invention can be contrasted with Su by seeing that the sequence of applicants' invention is as follows: Undope silicon glass (4) plus BPSG formation (6) plus PETEOS (38) plus planarization (cmp etch) plus second PETEOS (46). Su, therefore does not suggest the missing features from Kuo and applicants' admitted prior art. Indeed, he is expressly missing the layers as claimed in applicants' structure, and he certainly does not teach or suggest the missing feature of a second layer of PETEOS on top of and in contact with the BPSG layer

and also on top of and in contact with a first planarized PETEOS layer. These features are not found in nor are obvious from any combination of prior art.

The Examiner appears to make a rejection based completely on hindsight and without reference to any prior art in the remarks at the bottom of page 4, last full paragraph, and the top of page 5. The Examiner states that it would be obvious to one of ordinary skill in the art to remove PETEOS layer 22 to expose at least a portion of the BPSG layer which would then, according to the Examiner, obviously suggest an additional layer of PETEOS to be formed since removing portions of the first PETEOS layer would decrease the thickness of the premetal dielectric stack which would then decrease the aspect ratio of any subsequently formed contact opening. These suppositions by the Examiner are completely unwarranted and unsupported by the prior art. Clearly, no prior art shows these features. The Examiner seems to suggest that they would be obvious to one of ordinary skill in the art merely because it would be more desirable to make a more reliable device. However, no prior art is cited to support the Examiner's proposition of these particular layers. If the Examiner is going to maintain this rejection and the reasoning for the obviousness-type statement, reference to a particular piece of prior art is respectfully requested.

It is believe that these features are in fact not at all obvious. Applicants disagree that it would be obvious to one of ordinary skill in the art to perform the etching of the first layer of PETEOS until it exposes a portion of the BPSG layer. Nor would it be obvious to add the additional PETEOS layer which is in contact with both the first PETEOS layer and the BPSG layer. No prior art shows or even suggests as obvious the features stated by the Examiner as being obvious. Again, applicants disagree that such features would be obvious and believe that they are both novel and not obvious to any of skill in the art.

For example, the Examiner also cited in this Office Action a reference from Murao, U.S. Patent No. 5,518,962. As can be seen, he deposits two PETEOS layers, 130A and 131. However, he does not planarize the first PETEOS layer 130A until it exposes the BPSG layer 120. Thus, Murao teaches directly away from and the opposite of applicants' present invention by failing to planarize and etch the first layer 130A until it exposes the BPSG layer 120. Other prior art documents are equally deficient in this regard. Thus, applicants can only conclude that it would not be obvious to one of skill in the art, and there is no prior art with

which Kuo, Su et al., or even its own admitted prior art can be combined to render these features obvious.

In the second half of paragraph 14, on page 5, the Examiner notes that the specification contains no disclosure to the critical nature of the claimed features regarding the extent of etching to achieve planarization of the PETEOS layer. He concludes in the paragraphs that applicants must show that the chosen alternative elements are critical. Applicants strongly disagree. It is not a requirement of U.S. patent law, nor would it be expected that the specification of such semiconductor process technology contain statements regarding whether certain steps are of a critical nature. Such showing of "critical nature" is not a requirement for patentability. The present claimed structure is novel. The present claimed structure is not obvious in light of the prior art. There is no need for Applicants to provide statements in their own specification regarding the critical nature of any particular steps, nor is it desirable to do so in U.S. patent specifications. All that is required is that disclosure of the claimed invention be in a manner that would enable it to be manufactured, that it be in the inventor's best mode, and that it be novel and not obvious in light of the prior art. These are all met by applicants' disclosure and claims. Allowance of the claims is respectfully requested.

Applicants' U.S. attorney recently received the European search report. The European search report was issued June 19, 2000, and received by applicants' U.S. counsel on July 27, 2000, approximately a month later. Applicants are therefore submitting the European search report together with all art cited therein in an idea as attached herewith. Since applicants were not aware of the prior art until within the last few days, the fee for filing late prior art is not needed.

Applicants' attorney has reviewed the prior art from the European search report and does not see any prior art which is any more relevant than what the Examiner has found in the current U.S. search report. For example, applicants note that much of it is either not as relevant, or merely cumulative. The European search report contains, for example, the European version of the Murao patent previously cited by this Examiner. It contains other documents which are also not seen as any more relevant than those documents already considered by the U.S. Examiner.

Since the claims are clear and allowable over all prior art of record, allowance of all claims is respectfully requested.

Respectfully submitted,

Shin Hwa Li and Annie Tissier

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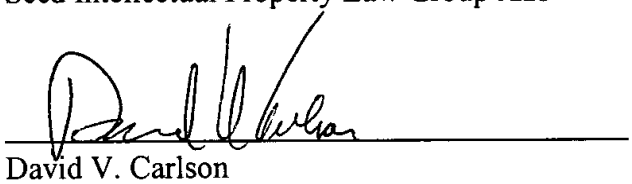

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